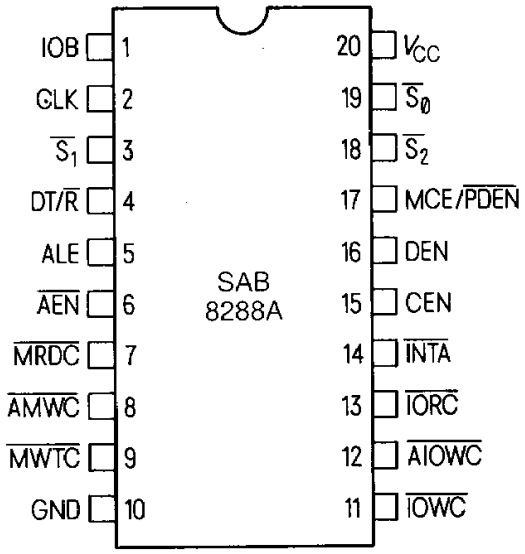
SIEMENS

Preliminary

SAB 8288A Bus Controller for SAB 8086 Family Processors

- Fully compatible with SAB 8288
- 40% Less Power Supply Current than Standard SAB 8288
- Bipolar Drive Capability
- Provides Advanced Commands
- Provides Wide Flexibility in System Configurations
- 3-State Command Output Drivers
- Configurable for Use with an I/O Bus
- Facilitates Interface to One or Two Multi-Master Busses

Pin Configuration



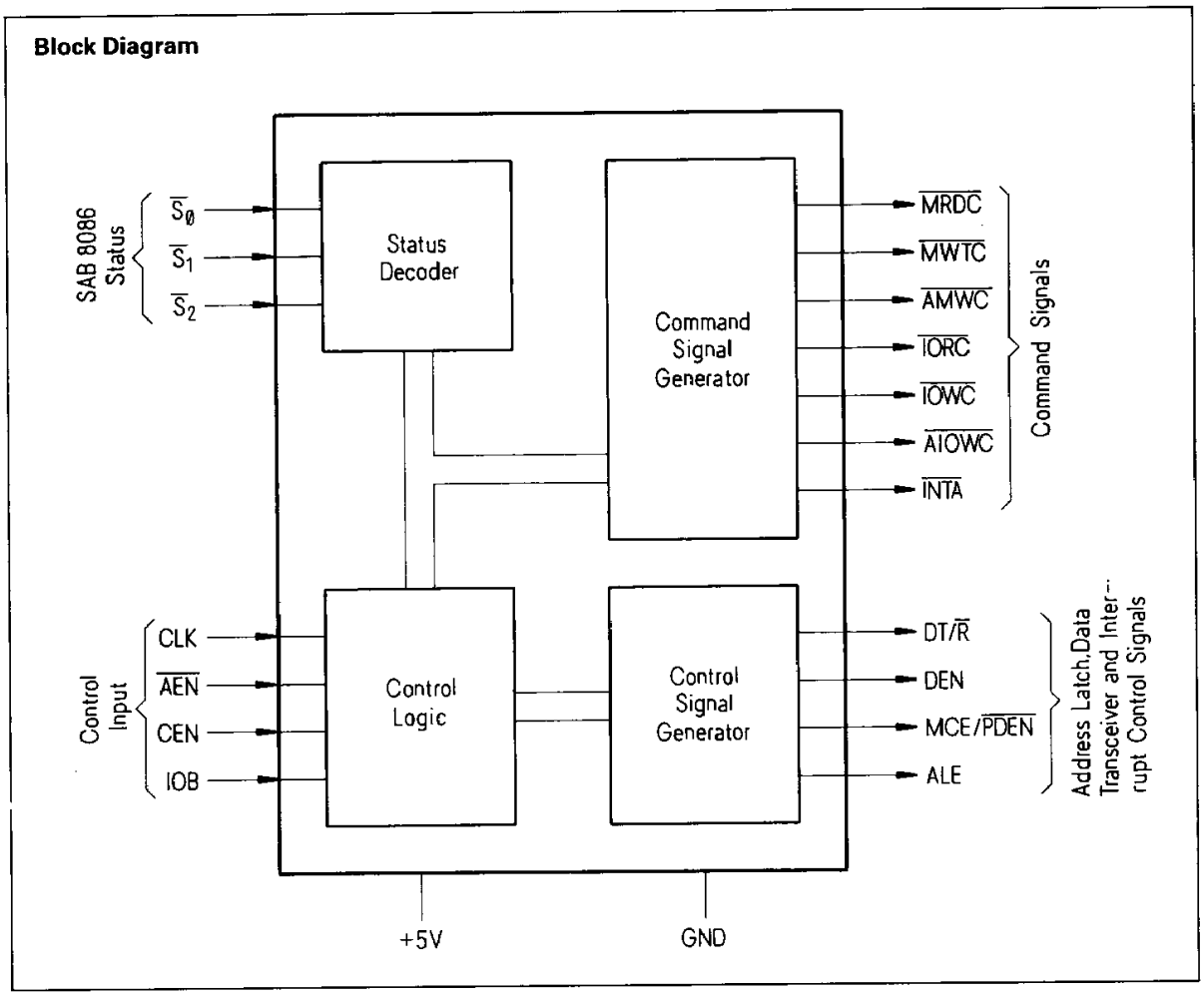
Pin Names

$\overline{S_0} - \overline{S_2}$	Status
CLK	Clock
ALE	Adress Latch Enable
DEN	Data Enable
DT/$\overline{R}$	Data Transmit/Receive
$\overline{AEN}$	Address Enable
CEN	Command Enable
IOB	Input/Output Bus Mode
$\overline{AIOWC}$	Advanced I/O Write
$\overline{IOWC}$	I/O Write
$\overline{IORC}$	I/O Read
$\overline{AMWC}$	Advanced Memory Write
$\overline{MWTC}$	Memory Write
$\overline{MRDC}$	Memory Read
$\overline{INTA}$	Interrupt Acknowledge
MCE/$\overline{PDEN}$	Master Cascade/Peripheral Data
V_{CC}	Power Supply (+5V)
GND	Ground (0V)

SAB 8288A Bus Controller is a 20-pin bipolar component for use with medium-to-large SAB 80186, SAB 80188, SAB 8086 and SAB 8088 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.
This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Block Diagram



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
IOB	1	I	INPUT/OUTPUT BUS MODE – When the IOB is strapped HIGH the SAB 8288A functions in the I/O Bus mode. When it is strapped LOW, the SAB 8288A functions in the System Bus mode. (See sections on I/O Bus and Systems Bus modes).
CLK	2	I	CLOCK – This is a clock signal from the SAB 8284A or SAB 8284B clock generator and serves to establish when command and control signals are generated.
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	3, 18, 19	I	STATUS INPUT PINS – These pins are the status input pins from the SAB 80186, SAB 80188, SAB 8086 or SAB 8088 processors. The SAB 8288A decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH. (See chart under Functional Description).

Symbol	Number	Input (I) Output (O)	Function
DT/$\overline{R}$	4	O	DATA TRANSMIT/RECEIVE – This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).
ALE	5	O	ADDRESS LATCH ENABLE – This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
$\overline{AEN}$	6	I	ADDRESS ENABLE – $\overline{AEN}$ enables command outputs of the SAB 8288A Bus Controller at least 105 ns after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the SAB 8288A is in the I/O Bus mode (IOB tied HIGH).
$\overline{MRDC}$	7	O	MEMORY READ COMMAND – This command line instructs the memory to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	ADVANCED MEMORY WRITE COMMAND – The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	MEMORY WRITE COMMAND – This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{IOWC}$	11	O	I/O WRITE COMMAND – This command line instructs an I/O device to read the data on the data bus. This signal is active LOW.
$\overline{AIOWC}$	12	O	ADVANCED I/O WRITE COMMAND – The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IORC}$	13	O	I/O READ COMMAND – This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{INTA}$	14	O	INTERRUPT ACKNOWLEDGE – This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
CEN	15	I	COMMAND ENABLE – When this signal is LOW all SAB 8288A command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
DEN	16	O	DATA ENABLE – This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
MCE/$\overline{PDEN}$	17	O	This is a dual function pin: MCE (IOB is tied LOW) – **Master Cascade Enable** occurs during an interrupt sequence and serves to read a Cascade. Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB is tied HIGH) – **Peripheral Data Enable** enables the data bus transceiver for the I/O bus during I/O instructions. It performs the same function for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.
V_{CC}	20	–	Power Supply (+5V)
GND	10	–	Ground (0V)

Functional Description

The command logic decodes the three SAB 80186, SAB 80188, SAB 8086 or SAB 8088 CPU status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) to determine what command is to be issued. This chart shows the meaning of each status "word".

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Processor State	SAB 8288A Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

The command is issued in one of two ways dependent on the mode of the SAB 8288A Bus Controller.

I/O Bus Mode – The SAB 8288A is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the SAB 8288A immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one SAB 8288A Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode – The SAB 8288A is in the System Bus mode if the IOB pin is strapped LOW. In this mode no command is issued until 115 ns after the $\overline{AEN}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command output are:
$\overline{MRDC}$ – Memory Read Command
$\overline{MWTC}$ – Memory Write Command
$\overline{IORC}$ – I/O Read Command
$\overline{IOWC}$ – I/O Write Command
$\overline{AMWC}$ – Advanced Memory Write Command
$\overline{AIOWC}$ – Advanced I/O Write Command
$\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the SAB 8288A are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enable onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the SAB 8288A. When the SAB 8288A is in the IOB mode (IOB HIGH) the PDEN signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the SAB 8288A is in the System Bus mode (IOB LOW). During any interrupt sequence there are two interrupt acknowledge cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{S}_0$, S_1, S_2) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the SAB 8288A. If the CEN pin is high the SAB 8288A functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

Absolute Maximum Ratings [1]

Temperature Under Bias	0 to +70 C
Storage Temperature	−65 to +150 C
All Output and Supply Voltages	−0.5 to +7 V
All Input Voltages	−1.0 to +5.5 V
Power Dissipation	1 W

D.C. Characteristics

T_A = 0 to 70 C; V_{CC} = +5 V ± 10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_C	Input Clamp Voltage		−1	V	I_C = −5 mA
I_{CC}	Power Supply Current	–	140	mA	All outputs open
I_F	Forward Input Current		0.7		V_F = 0.45 V
I_R	Reserve Input Current		50	µA	V_R = V_{CC}
V_{OL}	Output Low Voltage Command Outputs Control Outputs		0.5 0.5	V	I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage Command Outputs Control Outputs	2.4 2.4	–		I_{OH} = −5 mA I_{OH} = −1 mA
V_{IL}	Input Low Voltage	–	0.8		–
V_{IH}	Input High Voltage	2.0	–		
I_{OFF}	Output Off Current	–	100	µA	V_{OFF} = 0.4 to 5.25 V

A.C. Characteristics

T_A = 0 to 70 C; V_{CC} = +5 V ± 10%

Timing Requirements

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
t_{CLCL}	CLK Cycle Period	100		ns	–
t_{CLCH}	CLK Low Time	50			
t_{CHCL}	CLK High Time	30			
t_{SVCH}	Status Active Setup Time	35	–		
t_{CHSV}	Status Active Hold Time	10			
t_{SHCL}	Status Inactive Setup Time	35			
t_{CLSH}	Status Inactive Hold Time	10			
t_{ILIH}	Input, Rise Time	–	20		From 0.8V to 2.0V
t_{IHIL}	Input, Fall Time		12		From 2.0V to 0.8V

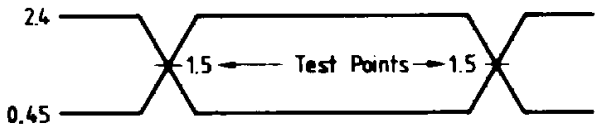
1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Timing Responses

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
t_{CVNV}	Control Active Delay	5	45	ns	
t_{CVNX}	Control Inactive Delay	10			
t_{CLLH}, t_{CLMCH}	ALE MCE Active Delay (from CLK)	–	20		
t_{SVLH}, t_{SVMCH}	ALE MCE Active Delay (from Status)				
t_{CHLL}	AIE Inactive Delay	4	15		$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
t_{CLML}	Command Active Delay	10	35		
t_{CLMH}	Command Inactive Delay				
t_{CHDTL}	Direction Control Active Delay	–	50		
t_{CHDTH}	Direction Control Inactive Delay		30		
t_{AELCH}	Command Enable Time		40		Other: I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 80 pF
t_{AEHCZ}	Command Disable Time				
t_{AELCV}	Enable Delay Time	115	200		
t_{AEVNV}	$\overline{AEN}$ to DEN	–	20		
t_{CEVNV}	CEN to DEN, PDEN		25		
t_{CELRH}	CEN to Command		t_{CLML}		
t_{OLOH}	Output, Rise Time		20		From 0.8V to 2.0V
t_{OHOL}	Output, Fall Time		12		From 2.0V to 0.8V

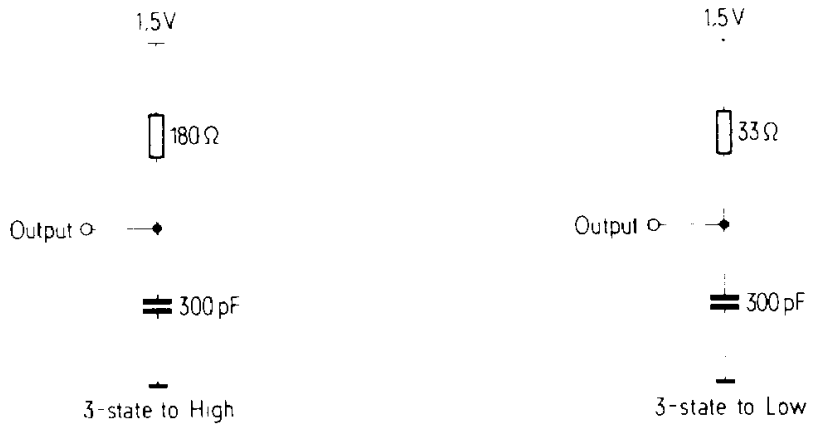
A.C. Testing Input, Output Waveform

Input/Output

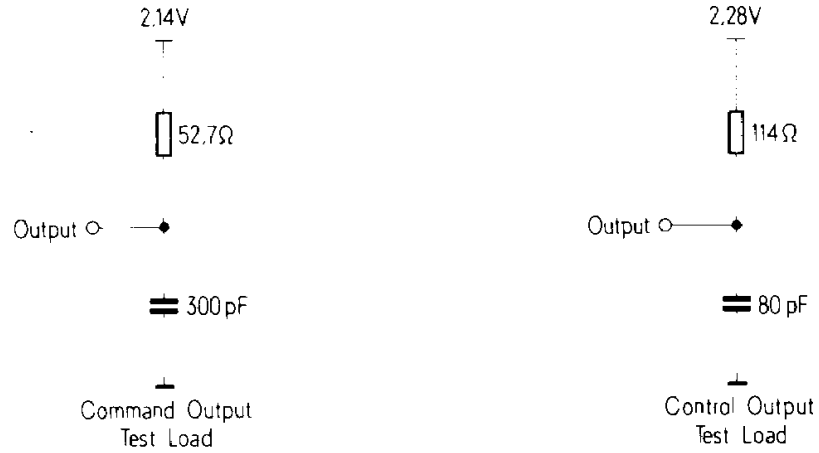


A.C. Testing Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". The clock is driven at 4.3V and 0.25V timing measurements are made at 1.5V for both a logic "1" and "0"

Test Load Circuits – 3-State Command Output Test Load

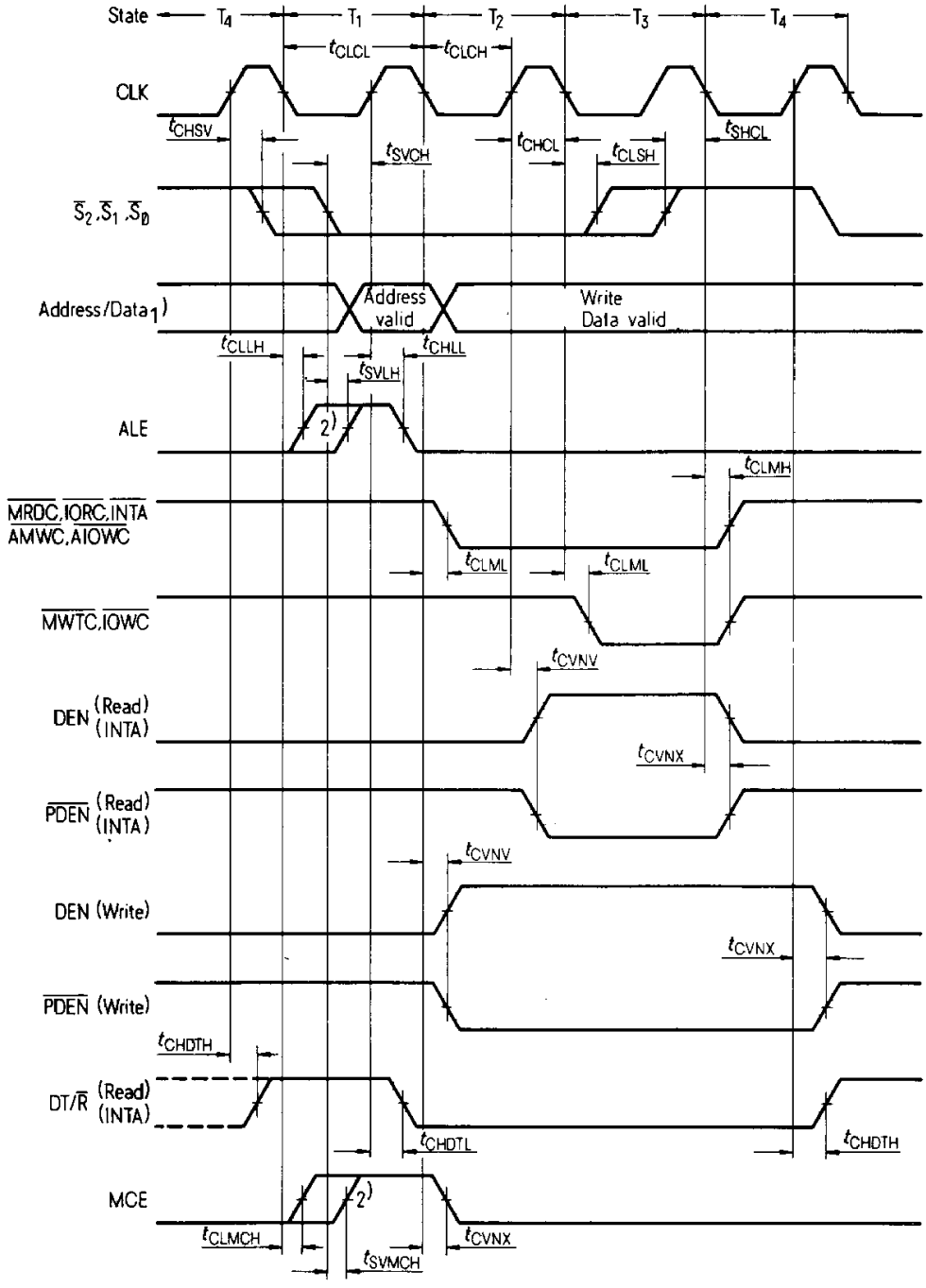


Test Load Circuits – 3-State Command Output Test Load



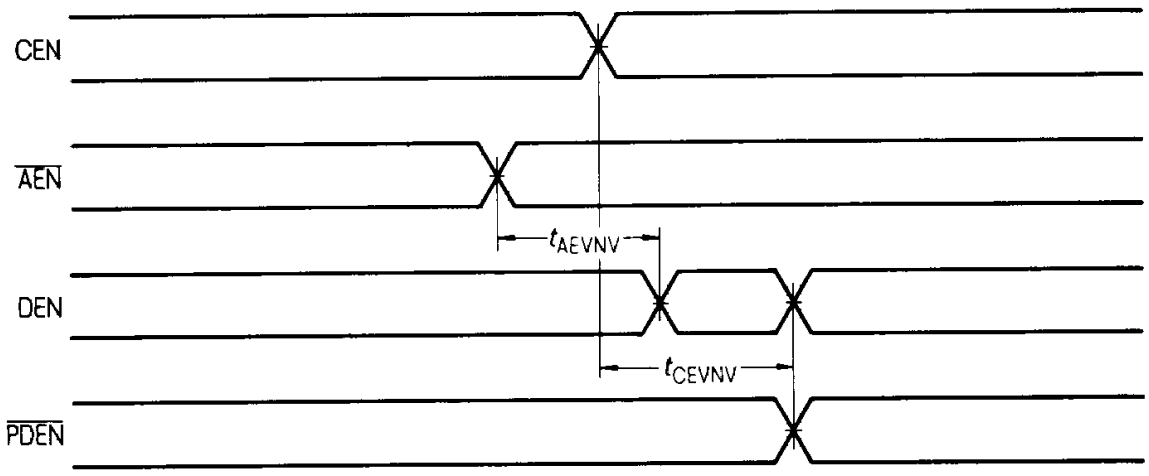
Waveforms

Timing Diagram

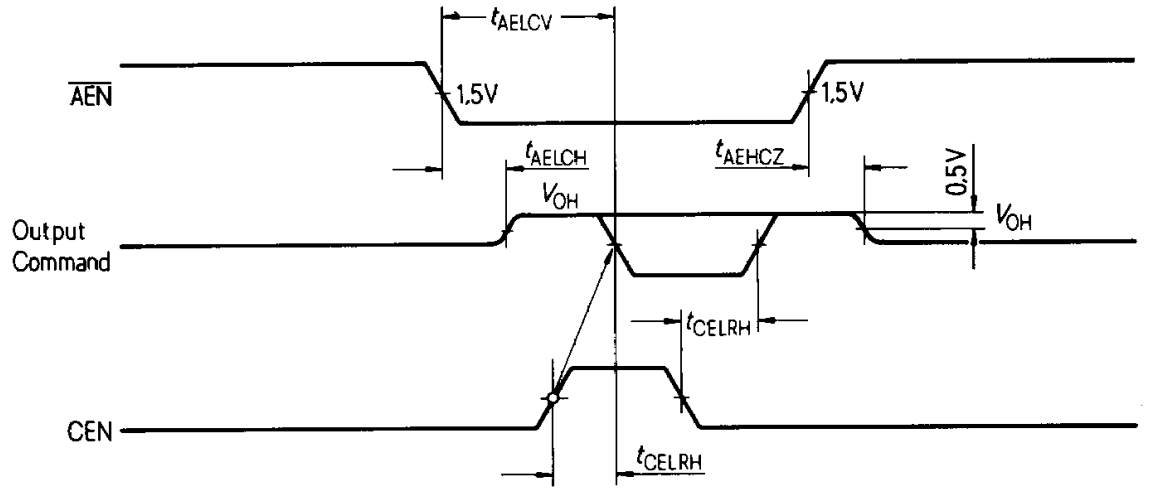


1) Address/Data Bus is shown only for reference purposes
2) Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.
3) All timing measurements are made at 1.5V unless specified otherwise.

DEN, PDEN Qualification Timing



Address Enable (AEN) Timing (3-State Enable/Disable)



CEN must be low or valid prior to T2 to prevent the command from being generated.

Ordering Information

Type	Description	Ordering code
SAB 8288A-P	Bus Controller (plastic)	Q 67020-Y 155