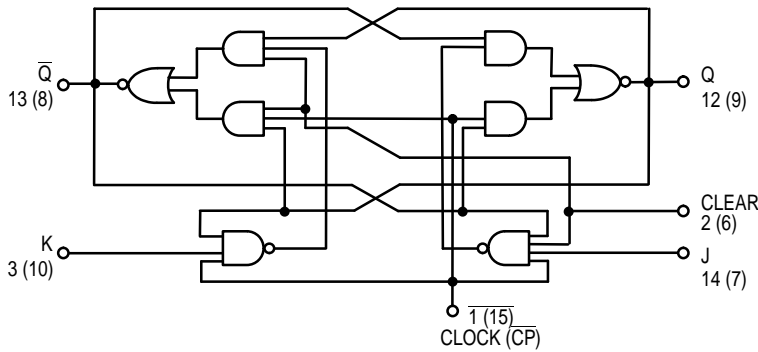




DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54LS/74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	\overline{C}_D	J	K	Q	\overline{Q}
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	\overline{q}	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	\overline{q}

H, h = HIGH Voltage Level

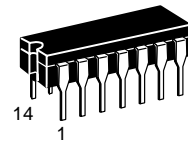
L, l = LOW Voltage Level

X = Don't Care

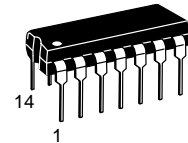
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

SN54/74LS73A

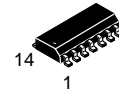
**DUAL JK NEGATIVE
EDGE-TRIGGERED FLIP-FLOP
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**

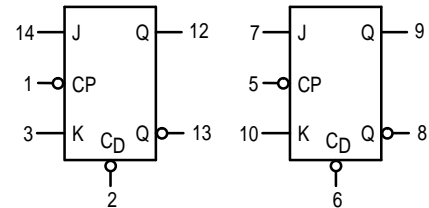


**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 4
GND = PIN 11

SN54/74LS73A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA I _{OL} = 8.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1 0.3 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	J, K Clear, Clock			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				6.0	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	45		MHz	Figure 1
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output		15	20	ns	Figure 1
			15	20	ns	

V_{CC} = 5.0 V
C_L = 15 pF

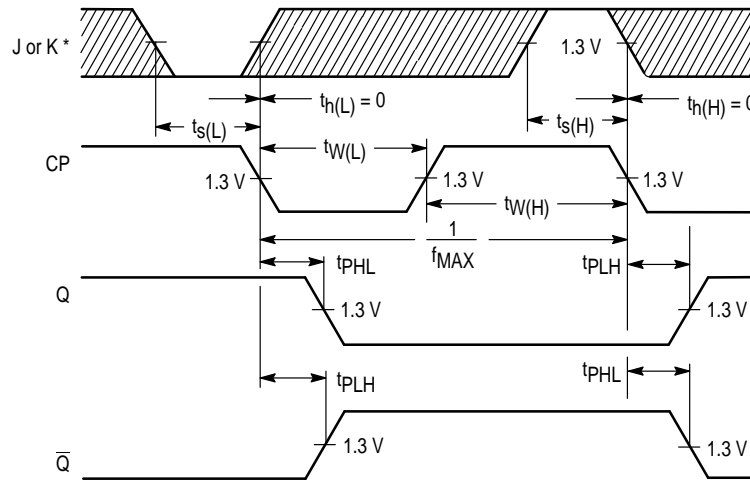
AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width High	20			ns	Figure 1
t _W	Clear Pulse Width	25			ns	Figure 2
t _s	Setup Time	20			ns	Figure 1
t _h	Hold Time	0			ns	

V_{CC} = 5.0 V

SN54/74LS73A

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width

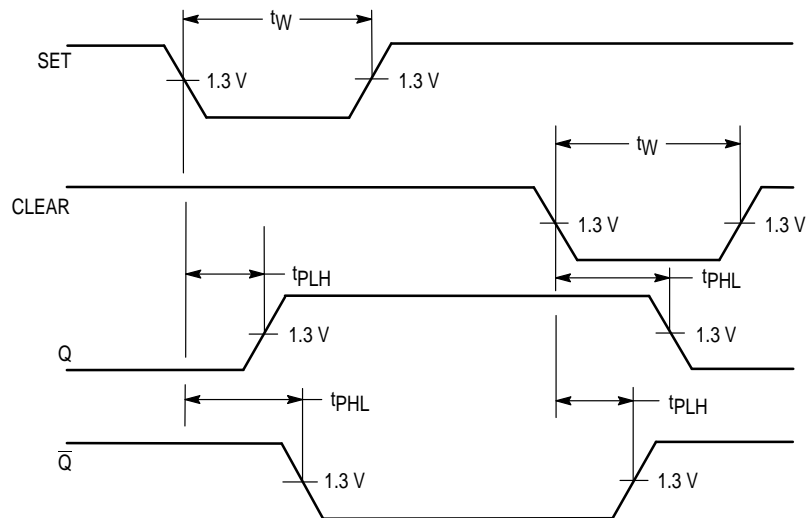


Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths